# Technologie Evolutives et Disruptives pour les prochaines générations de cellules solaires Silicium

M. Despeisse, on behalf of CSEM and EPFL/pvlab research teams

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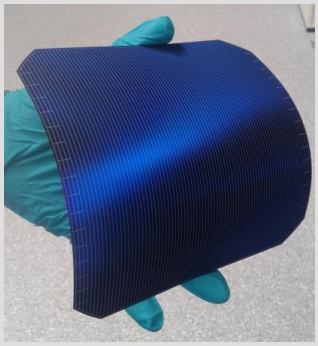
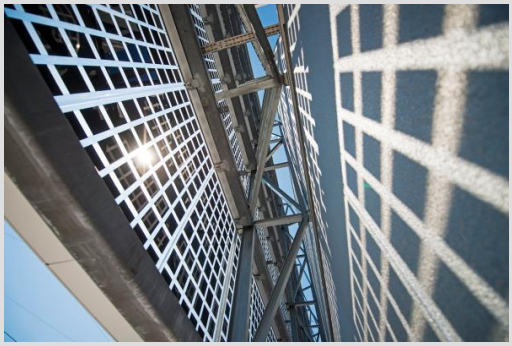
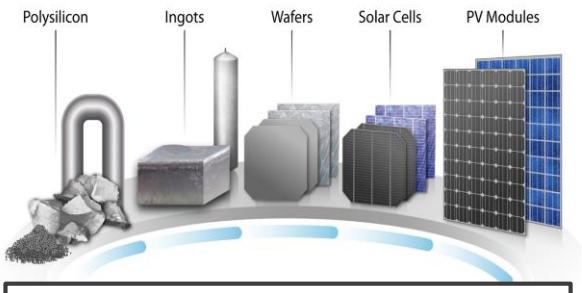
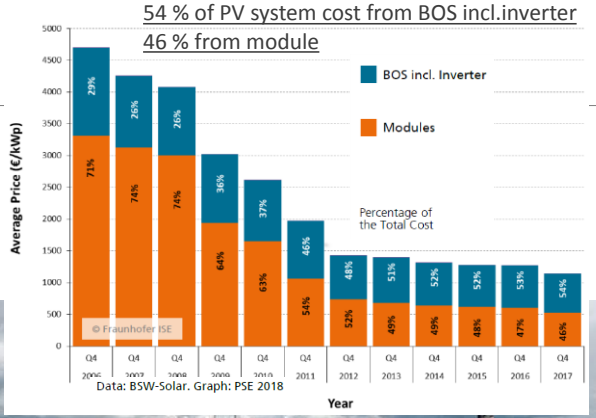




## HIGH PERFORMANCE LOW COST




54 % of PV system cost from BOS incl.inverter
46 % from module




**MATERIALS, PROCESSES and TECHNOLOGIES For COST-COMPETITIVE MANUFACTURING**

***Low $/Wp***

**HIGH EFFICIENCY**

**HIGH FIELD PERFORMANCE**

***Low $/kWh***

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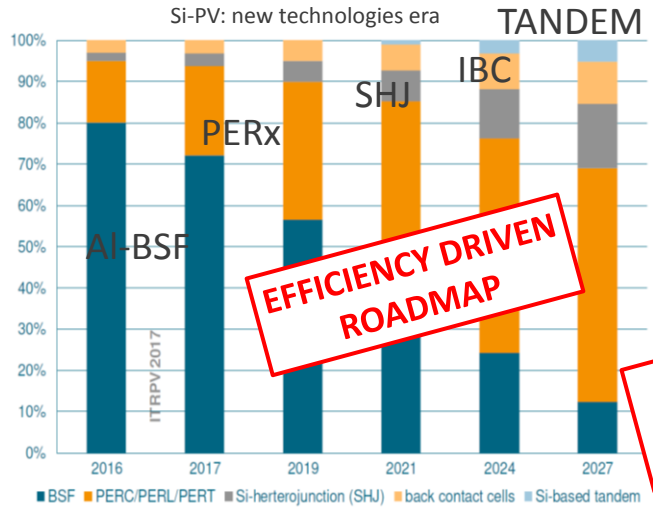
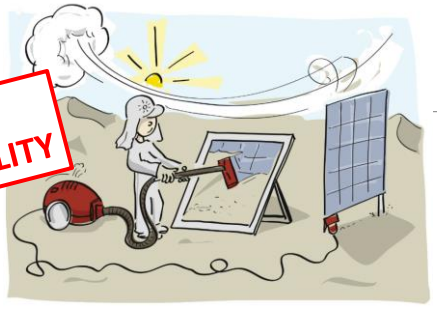
## HIGH PERFORMANCE LOW COST

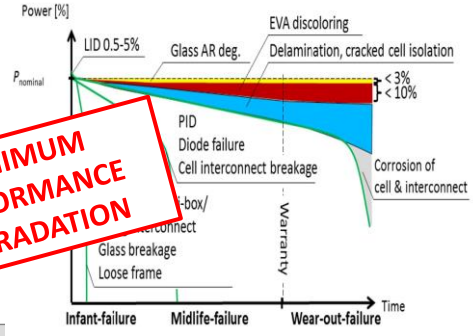



HIGH BIFACIALITY

EFFICIENCY DRIVEN ROADMAP

MINIMUM PERFORMANCE DEGRADATION

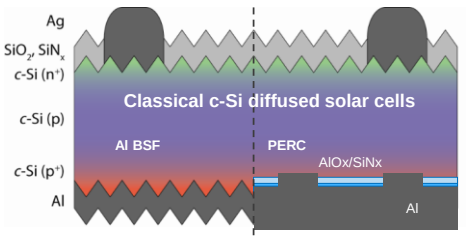




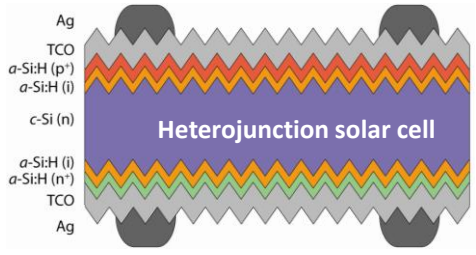



## STEP 1: IMPLEMENTING PASSIVATING CONTACTS & GOING BIFACIAL

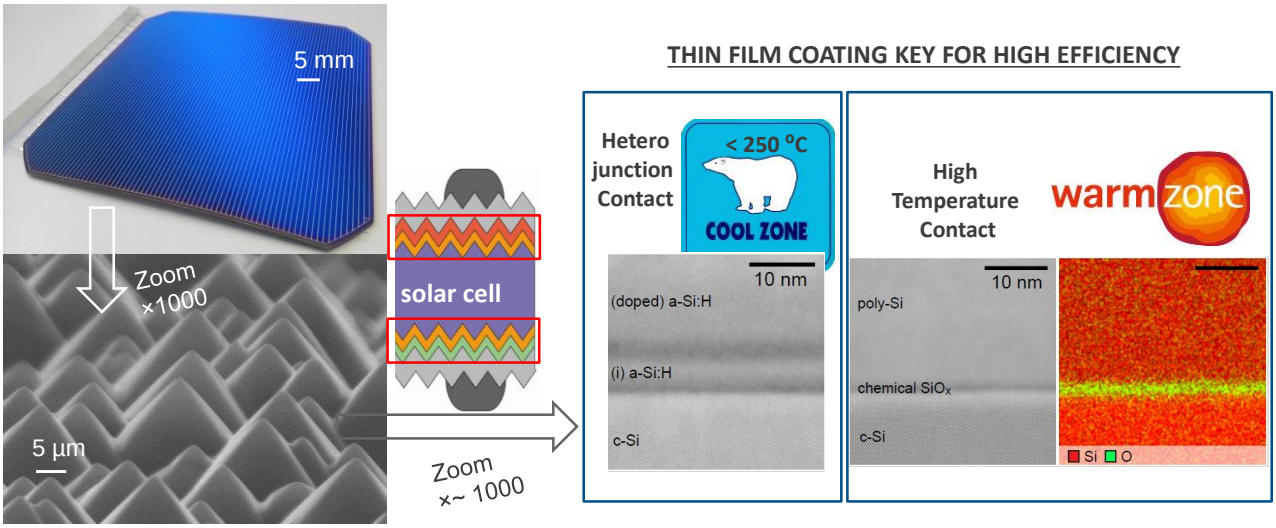
Direct contact between c-Si and metal
**Recombinative contact**
→ Lower operating voltage & $V_{oc}$




Heterocontact between c-Si and metal
**Passivating contacts**
→ Higher operating voltage & $V_{oc}$
**Bifacial structure**

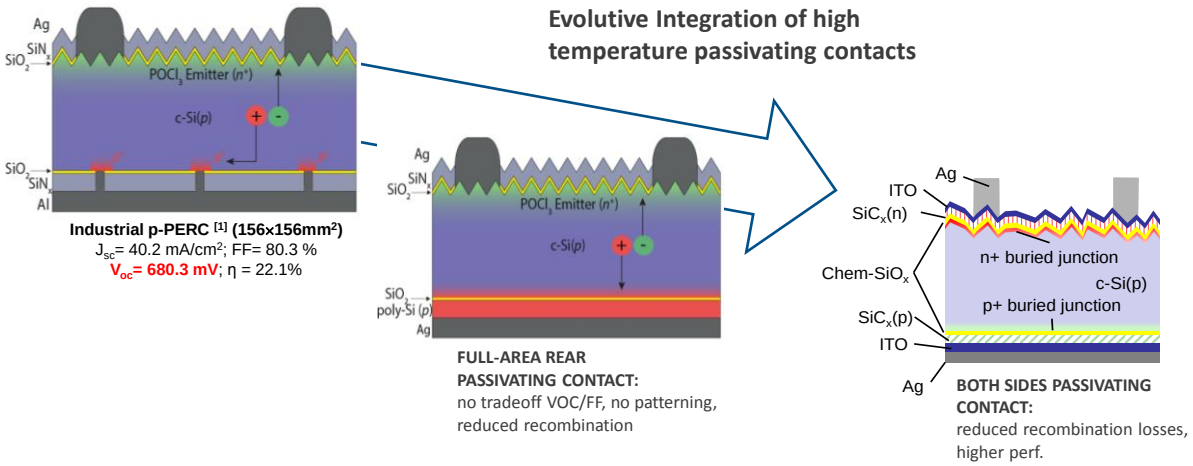


## STEP 1: IMPLEMENTING PASSIVATING CONTACTS & GOING BIFACIAL





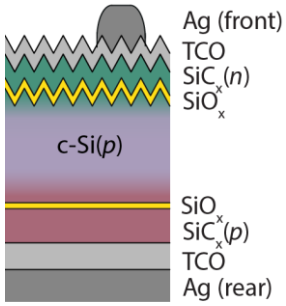

## STEP 1: IMPLEMENTING PASSIVATING CONTACTS & GOING BIFACIAL

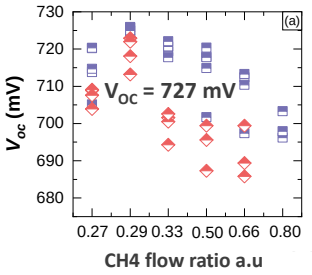


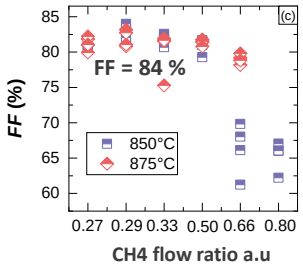
## STEP 1: IMPLEMENTING PASSIVATING CONTACTS & GOING BIFACIAL

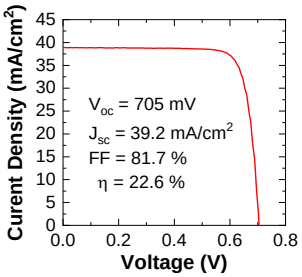
**SiOx/SiCx high temperature passivating contacts developed in EPFL/CSEM:**
high operating voltages FF up to 84 %, $V_{OC}$ of 727 mV on flat wafers :
high passivation, low transport losses achieved.

**Target: achieve similar properties on textured surfaces + limit front-side parasitic absorption.**



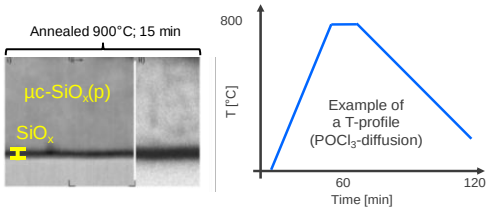

*See poster of Josua Stuckelberger - EPFL*



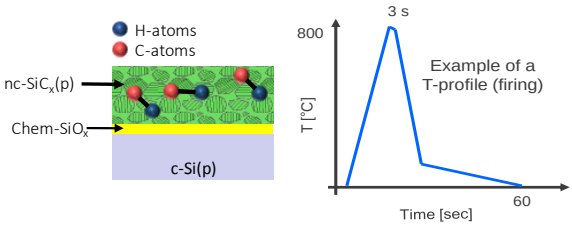
## STEP 1: IMPLEMENTING PASSIVATING CONTACTS & GOING BIFACIAL

**TOWARDS LEAN PROCESS FLOW INTEGRATION of HIGH TEMPERATURE PASSIVATING CONTACTS**

**Approach 1:**
**Co-annealing with $POCl_3$ process for emitter formation**




**Approach 2:**
**Co-firing with front side Ag-paste**



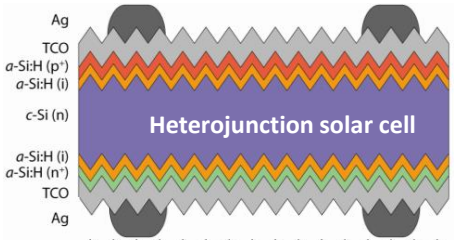

*See poster of Josua Stuckelberger - EPFL*

## 1 : PASSIVATING CONTACTS & BIFACIAL

> 24 % R&D level | CAPEX reduction | Metallization/ Interco costs | Mass prod. demo | Upgrade roadmap | Capitalize on Tcoeff, bifacial, thin wafer

**DISRUPTIVE APPROACH : SILICON HETEROJUNCTION**
**LEAN PROCESS FLOW, HIGH PASSIVATION**

| Chemical baths | PECVD | PVD | Metallization |
|---|---|---|---|
| c-Si surface preparation | a-Si:H thin films deposition, intrinsic and doped: i-n, i-p | TCO | Screen printing + curing at 200° C |




Silicon HETEROJUNCTION Cells and Modules R&D platforms established at CSEM



## 1 : PASSIVATING CONTACTS & BIFACIAL

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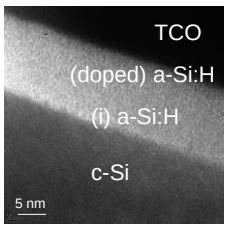
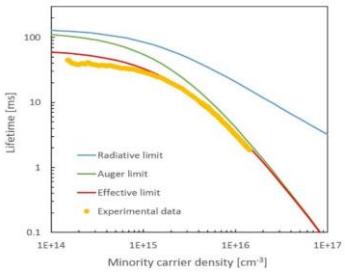
Best cell produced so far in CSEM:

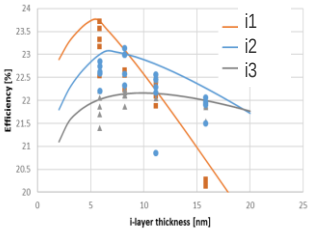
**24.1 %**

**$V_{OC}$ = 727 mV,**
**$J_{SC}$ = 40.8 mA/cm2,**
**FF = 81.1 %**

**Processes for a-Si:H deposition key to achieve required opto-electronic properties.**



## 1 : PASSIVATING CONTACTS & BIFACIAL

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**HIGH EFFICIENCY in PILOT PRODUCTION**

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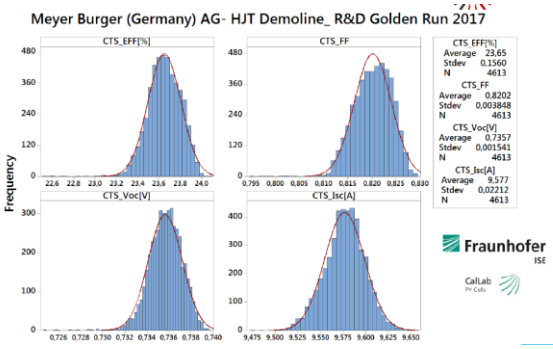


**24.02%**
highest cell efficiency
**23.7%**
average efficiency
**335W**
module power (mono facial)

Fraunhofer ISE CalLab PV Cells

TÜVRheinland



## 1 : PASSIVATING CONTACTS & BIFACIAL

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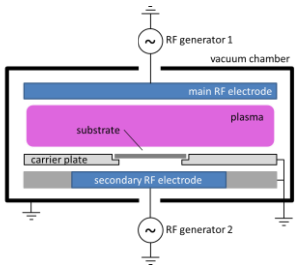
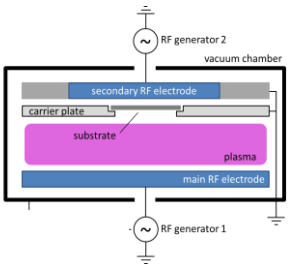
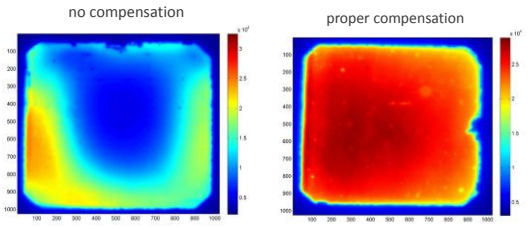
SWISS MADE INDEOtec PLASMA PROCESS EQUIPMENT

Alternative PECVD reactor :
MIRROR Concept: Both-sides deposition without vacuum break/no flipping of wafer
Cross contamination management: i/n in 1 reactor, i/p in 1 reactor
Parallelism



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**SMARTWIRE TECHNOLOGY BENEFITS**

Less shading
Less resistivity losses
Cell paste usage reduction (up to 70%)
Better resistance for micro cracks
Low temperature and low thermal stress interconnection technology
No alignment needed (≠ MBB)
Aesthetically attractive

**Front** 25 mg

BBless

**Ag cost = 1.3 $cent/cell**

**Front** 125 mg

5BB

**Ag cost = 6.8 $cent/cell**



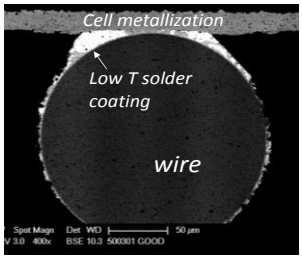
## 1 : PASSIVATING CONTACTS & BIFACIAL

> 24 % R&D level | CAPEX reduction | Metallization/ Interco costs | Mass prod. demo | Upgrade roadmap | Capitalize on Tcoeff, bifacial, thin wafer

**NEW GENERATION SMARTWIRE**

Cost decrease in wires : Indium-free low temperature alloy coating on wires
Performance increase : + 2% from new design & UV-through

Demonstration of metallurgical bonding btw. HJT cell finger and a wire w. selected Indium free low T solder satisfying above criteria.



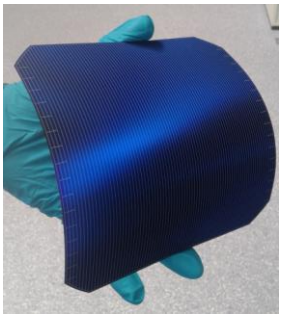


**Reliability (HJT):**
PTC < 1% degradation after 3xIEC
DH < 2% degradation after 3xIEC
**Reliability (PERC):**
PTC < 1% degradation after 3xIEC
DH < 3% degradation after 2xIEC

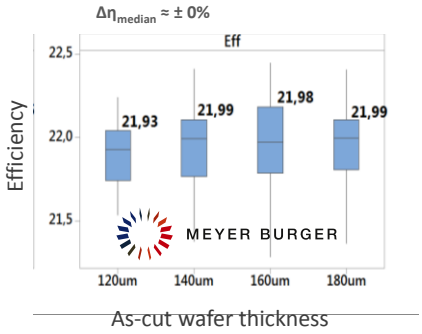
## 1 : PASSIVATING CONTACTS & BIFACIAL

> 24 % R&D level | CAPEX reduction | Metallization/ Interco costs | Mass prod. demo | Upgrade roadmap | Capitalize on Tcoeff, bifacial, thin wafer

p-type wafer 180µm: ~ 62 $cts/wafer
n-type wafer 180µm: ~ 68 $cts/wafer
**Cost decrease w. thickness: 1.5 $cts/10 µm**
**n-type wafer 120µm: ~ 59 $cts/wafer**



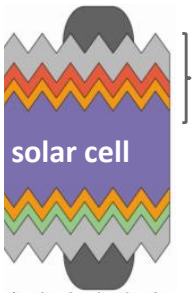
Thin wafer integration in production: potential for down to 120 µm as-cut demonstrated by Meyer Burger.
- Excellent surface passivation permits no performance loss ($J_{SC}$ loss, $V_{OC}$ gain).
- Bifacial structure equilibrates stress on both cell sides.



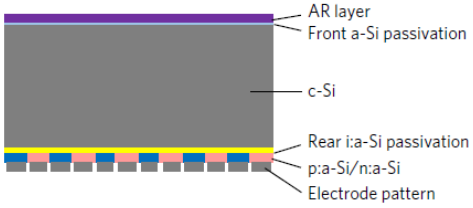



## 2 : BACK CONTACTS w. PASSIVATING CONTACTS

Upgrade roadmap → **BACK CONTACT**

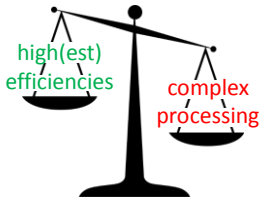



Front-side current loss:
Parasitic absorption




Highest efficiency potential demonstrated:
world record – Kaneka / 26.6 %
*[K. Yoshikawa, Nature Energy 2, 17032 (2017)]*

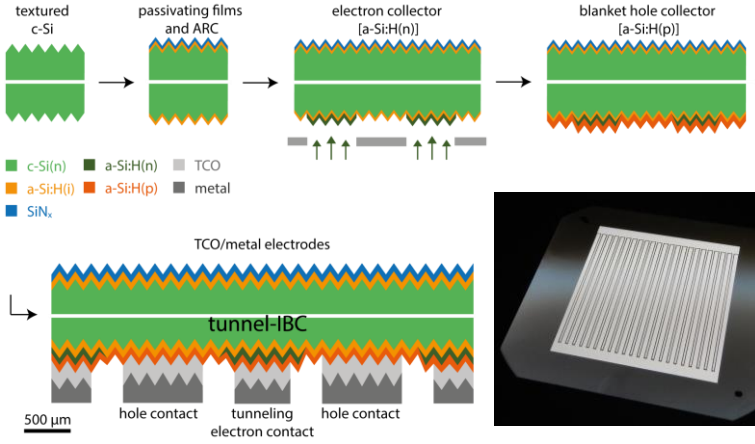
Challenge for cost-effective manufacturing keeping high efficiency.




**«TUNNEL IBC-HJT» concept**

EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE :: csem

## 2 : BACK CONTACTS w. PASSIVATING CONTACTS




SIMPLE PROCESS FLOW
MINIMIZATION OF MATERIALS
**HIGH EFFICIENCY demonstrated so far up to 24.1 %**

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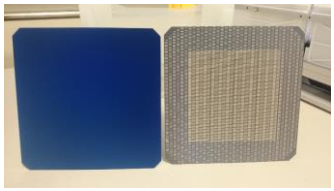
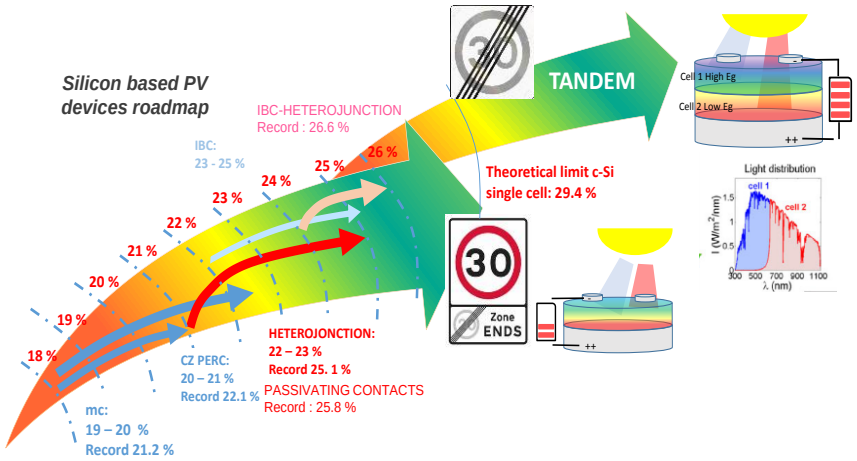
Transfer to full wafer industrial processing.





## EFFICIENCY DRIVEN TECHNOLOGY UPGRADE



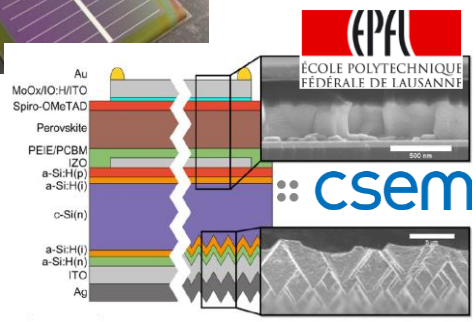
## 3 : SILICON BASED TANDEM CELLS


### III-V/Si

**World records:**
**32.8 % 4-terminal tandem III-V on Silicon HJT.**
**35.9 % 4-terminal triple junction III-V on Silicon HJT**

- Breakthrough in III-V manufacturing with drastic costs reduction
- New Integration approach
- Alternative top cell material w. low cost potential

### PEROVSKITE/Si




**> 25 % certified efficiency for monolithic PK/Si tandem achieved at EPFL/CSEM**

*See poster of Quentin Jeangros - EPFL*



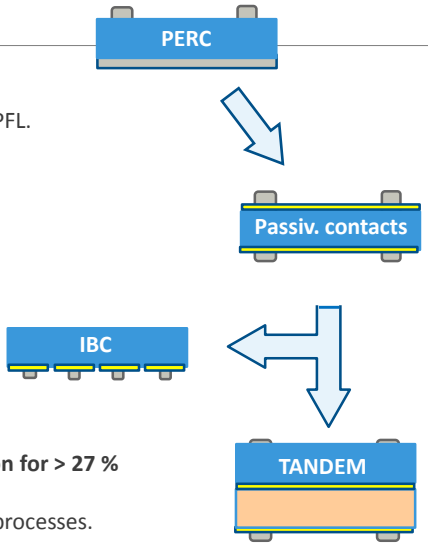
## CONCLUSION

**PASSIVATING CONTACTS to extend cell efficiency > 24 %**:
High temperature approaches w. SiOx/SiCx developed at CSEM/EPFL.
High electrical properties. Lean process flow to demonstrate.

Silicon Heterojunction w. > 24 % at CSEM.
Simple process flow, thin wafers, bifacial, lowest LCOE. Advanced manufacturing developed w. Swiss industry.

**BACK CONTACTS to extend cell efficiency > 25-26 %**:
Simple process flow «TUNNEL-IBC» developed at CSEM/EPFL.
In transfer to Swiss industry.

**Perovskite as add-on technology to Silicon for > 27 %**
> 25 % demonstrated by EPFL/CSEM.
Work on higher eff., reliability, industrial processes.



## Thank you to all colleagues & partners

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MEYER BURGER

SWISS MADE INDEOtec PLASMA PROCESS EQUIPMENT

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

**Bundesamt für Energie BFE**
**Office fédéral de l'énergie OFEN**

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

Swiss Confederation

**Innosuisse – Swiss Innovation Agency**

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

Département fédéral de l'économie, de la formation et de la recherche DEFR
**Secrétariat d'Etat à la formation, à la recherche et à l'innovation SEFRI**



## Thank you for your attention

*CSEM PV Facade HJT cells*
*«Solar Visualised in Europe Award»*

*SmartWire*
*Heterojunction*
*PV facade*
*CSEM*